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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/781,125	02/18/2004	Christopher S. Johnson	400.149US02	3355
7590 10/27/2004			EXAMINER	
Leffert Jay & Polglaze, P.A.			LE, THONG QUOC	
P.O. Box 581009 Minneapolis, MN 55458-1009			ART UNIT	PAPER NUMBER
			2818	
			DATE MAILED: 10/27/2004	

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)			
	10/781,125	JOHNSON, CHRISTOPHER S.			
Office Action Summary	Examiner	Art Unit			
	Thong Q. Le	2818			
The MAILING DATE of this communication a Period for Reply	ppears on the cover sheet with the o	correspondence address			
A SHORTENED STATUTORY PERIOD FOR REF THE MAILING DATE OF THIS COMMUNICATION  - Extensions of time may be available under the provisions of 37 CFR after SIX (6) MONTHS from the mailing date of this communication.  - If the period for reply specified above is less than thirty (30) days, a r  - If NO period for reply is specified above, the maximum statutory period.  - Failure to reply within the set or extended period for reply will, by stat Any reply received by the Office later than three months after the ma earned patent term adjustment. See 37 CFR 1.704(b).	N. 1.136(a). In no event, however, may a reply be tireply within the statutory minimum of thirty (30) day of will apply and will expire SIX (6) MONTHS from tute, cause the application to become ABANDONE	mely filed ys will be considered timely. Ithe mailing date of this communication. ED (35 U.S.C. § 133).			
Status					
1) Responsive to communication(s) filed on					
	his action is non-final.				
3) Since this application is in condition for allow					
Disposition of Claims					
4) ☐ Claim(s) 1-44 is/are pending in the application 4a) Of the above claim(s) is/are withd 5) ☐ Claim(s) is/are allowed. 6) ☐ Claim(s) 1-44 is/are rejected. 7) ☐ Claim(s) is/are objected to. 8) ☐ Claim(s) are subject to restriction and	rawn from consideration.				
Application Papers					
9) The specification is objected to by the Examiner.					
10) The drawing(s) filed on is/are: a) accepted or b) objected to by the Examiner.					
Applicant may not request that any objection to the	<del>-</del> ,,	• •			
Replacement drawing sheet(s) including the corr 11) The oath or declaration is objected to by the	* * * * * * * * * * * * * * * * * * * *	•			
Priority under 35 U.S.C. § 119					
<ul> <li>12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).</li> <li>a) All b) Some * c) None of:</li> <li>1. Certified copies of the priority documents have been received.</li> <li>2. Certified copies of the priority documents have been received in Application No.</li> <li>3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).</li> <li>* See the attached detailed Office action for a list of the certified copies not received.</li> </ul>					
Attachment(s)  1)   Notice of References Cited (PTO-892)	4) 🔲 Interview Summary	/ (PTO-413)			
2) Notice of Draftsperson's Patent Drawing Review (PTO-948) 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/6 Paper No(s)/Mail Date	Paper No(s)/Mail D				

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#### **DETAILED ACTION**

1. Claims 1-44 are presented for examination.

#### Information Disclosure Statement

- This office acknowledges receipt of the following items from the Applicant:
   Information Disclosure Statement (IDS) filed on February 18,2004.
- 3. Information disclosed and list on PTO 1449 was considered.

## Claim Rejections - 35 USC § 112

- 4. The following is a quotation of the second paragraph of 35 U.S.C. 112:
  The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.
- 5. Claim 30 recites the limitation "the mode register" in line 5. There is insufficient antecedent basis for this limitation in the claim.
- 6. Claim 31 recites the limitation "the mode register" in line 3. There is insufficient antecedent basis for this limitation in the claim.
- 7. Claims 30-34 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. The omitted structural cooperative relationships are: the mode register.

The connection of mode register in claim does not disclosed.

Claims are required to amend for clarity.

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### Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

9. Claims 1-44 are rejected under 35 U.S.C. 102(e) as being anticipated by Nobunaga et al. (U.S. Patent No. 6,304,510).

Regarding claims 1-37, Nobunaga et al. disclose a system (Figure 1), comprising:

a controller (200); and

a memory device (100) coupled to the controller to receive signals therefrom, and comprising:

an array of memory cells (104) arranged in a plurality of addressable banks (bank 1, bank 2, bank 3, bank 4), each bank comprises addressable rows and columns of memory cells;

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a mode register (130); and

address circuitry (112,115,117) coupled to the mode register to configure the addressable banks in response to a program state of the mode register.

More specifically, Nobunaga et al. disclose wherein the addressable banks can be configured as either four or eight banks (Figure 1, bank1-4), and wherein the address circuitry selectively routes address signal to either a row decoder (118) or a bank decoder in response to the mode register, and column decoder (122) as claim 9 discloses, and a logic circuit (130) as claim 12 disclose.

Regarding claims 38-44, the apparatus discussed above would perform the method in claims 38-44. More specifically, Nobunaga et al. disclose this operating a memory device (Column 10, lines 45-64).

10. Claims 16-29, 35-44 are rejected under 35 U.S.C. 102(e) as being anticipated by Zitlaw et al. (U.S. Patent No. 6,549,468).

Regarding claim 16-29, 35-37, Zilaw et al. disclose a system, (Figure 1) comprising: a controller (201); and

a memory device (100) coupled to the controller to receive signals including an input signal therefrom, and comprising:

an array of memory cells (102) arranged in a plurality of addressable banks, each bank comprises addressable rows and columns of memory cells;

a decode circuit (116) to decode the input signal; and

an address circuitry (112) coupled to the decode circuit to configure the addressable banks in response to a program state of the input signal.

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More specifically, Zilaw et al. disclose wherein the addressable banks can be configured as either four or eight banks (Figure 1, 104,106,108,110), and wherein the address circuitry selectively routes address signal to either a row decoder (Figure 1, 114) or a bank decoder (116) in response to the input signal (Figure 1), and wherein the input signal is a one-bit binary input, and wherein the input signal is a multi-bit binary input and the number of banks is configurable (Figure 1), and wherein the address circuitry comprises a multiplex circuit (Figure 4) as claim 26 disclosed.

Regarding claims 38-44, the apparatus discussed above would perform the method in claims 38-44.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thong Q. Le whose telephone number is 571-272-1783. The examiner can normally be reached on 8:00am-5:00pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David C. Nelms can be reached on 571-272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thong Q. Le Primary Examiner Art Unit 2818

THONG LET PRIMARY EXAMINER